REMARKS

Claims 16-34, 36-40, and 43-52 have been canceled. Thus, claims 1-15, 35, 41-42, and 53 are pending in the present application.

In the Office Action, claims 1-2, 5-17, 21-24, 27-28, 32-34, 45-46, and 50-52 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Gafken (U.S. Patent No. 6,026,016). Claims 3-4, 18-20, 35, 41-42, and 53 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gafken in view of Short, "Embedded Microprocessor Design." Claims 16-24, 27-28, 32-34, 45-46, and 50-52 have been canceled, rendering the Examiner's rejections of these claims moot. The Examiner's remaining rejections are respectfully traversed.

Independent claims 1, 35, 41-42, and 53 set forth enable bits associated with a hardware debugging mode. The enable bits may be stored in a register and reset by a control logic. Claims 35, 41-42, and 53 set forth enable bits associated with a hardware debugging mode that may be stored in a register and reset by a control logic and associated enable lock bits. Hardware debugging modes are known in the art. For example, Advanced Micro Devices, Inc. provides a hardware debugging interface called the Hardware-Debug-Test (HDT) mode, which is based on the JTAG protocol. Other examples of hardware debugging interfaces include the background debug mode (BDM) provided by Motorola and the common on-chip processor (COP) provided by IBM.

In one embodiment of the present invention, the hardware debugging mode, such as the HDT mode, may be enabled or disabled based on one or more enable bits. For example, an HDT enable register 3115 is configured to store one or more HDT enable bits signifying whether HDT mode is enabled or disabled. The HDT reset logic 3120 is configured to set the one or more HDT enable bits to a default state upon a reset of the processor 805. Multiple embodiments for

controlling the HDT modes are contemplated, such as those illustrated in Figs. 20A and 20B. In one embodiment, the HDT mode is enabled as the default on non-production processors 805 used for engineering and testing. The HDT mode may be disabled as the default in standard production processors 805. In another embodiment, illustrated in Fig. 20A, the default state may be stored in and read from the NVRAM 3130. In this embodiment, the default state may be changeable, but in the illustrated embodiment, the default state is set to disabled. In still another embodiment, illustrated in Fig. 20B, the default state is set using a strapping option. The default value is provided to the HDT reset logic 3120B through the pull-up (or pull-down) resistor 3145. See Patent Application, page 65, line 17 – page 66, line 5.

In contrast, Gafken describes a lock bit array 705 that includes a read lock bit, which may prevent a corresponding block from being accessed in response to a memory read operation directed to that block. See Gafken, Figure 7 and related discussion. However, Gafken is completely silent with regard to hardware debugging and therefore fails to teach or suggest enable bits for a hardware debugging mode. Accordingly, Applicant submits that the invention set forth in claims 1, 35, 41-42, 53, and all claims depending therefrom is not anticipated by Gafken.

For at least the aforementioned reasons, Applicant requests that the Examiner's rejections of claims 1-2 and 5-15 under 35 U.S.C. 102(b) be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of the prior art of record. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Gafken is completely silent with regard to enable bits for a hardware debugging mode, as set forth in claims 1, 35, 41-42, and 53.

The Examiner relies upon Short to describe using non-volatile memory to store data. However, Short fails to remedy the fundamental deficiencies of the primary reference. Neither Gafken nor Short is at all concerned with hardware debugging and therefore these references fail to teach or suggest enable bits for a hardware debugging mode, as set forth in claims 1, 35, 41-42, and 53. Accordingly, Applicant respectfully submits that the cited references also fail to provide any suggestion or motivation to modify the prior art of record to arrive at the claimed invention.

For at least the aforementioned reasons, Applicant respectfully submits that the present invention is not obvious over Gafken and Short, either alone or in combination. Applicant requests that the Examiner's rejections of claims 3-4, 35, 41-42, and 53 under 35 U.S.C. 103(a) be withdrawn.

In the Office Action, claims 25-26, 29-30, 36, 43-44, and 47-48 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Yishay (U.S. Patent No. 5,704,039). Claims 31, 37-40, and 49 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yishay in view of Kime, "Logic and Computer Design Fundamentals." Claims 25-26, 29-31, 36-40, 43-44, and 47-49 have been cancelled, rendering the Examiner's rejections of these claims moot.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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